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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,782	03/31/2004	Kiyoshi Mita	14225-049001 / F1040149US	5223

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EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 06/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/813,782	MITA, KIYOSHI	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 12* is/are pending in the application.

4a) Of the above claim(s) *4 and 5* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 3 and 6 - 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on March 6, 2006 has been received and entered in the case.

Election/Restrictions

2. Claims 4 and 5 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected group II, there being no allowable generic or linking claim. Election was made without traverse in the reply filed on January 18, 2005.

3. It is suggested that applicants cancel claims 4 and 5 in response to this Office action.

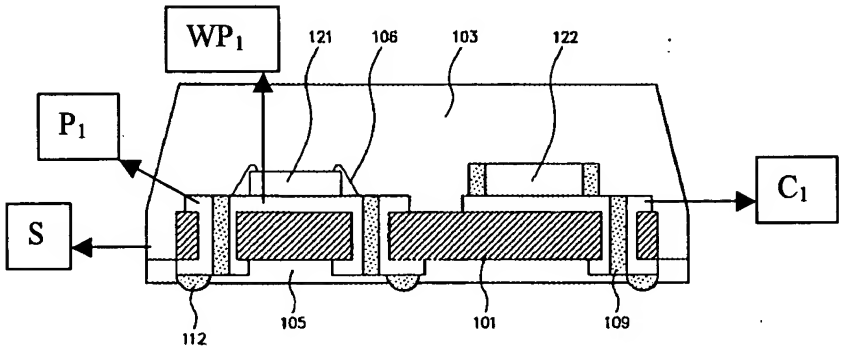
Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 – 3 and 6 – 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Takeda (U. S. Pat. No. 6,014,318).

Regarding claim 1, Takeda discloses in e.g., Fig. 4 a semiconductor device (the device in Fig. 4), comprising:



- a mounting substrate (101 and 105; see Fig. 4 and column 1, lines 33 – 38) having a first main surface (the surface where the sealing resin 103 are formed) and a second main surface (the surface where the sealing resin 103 are not formed) opposite the first main surface (see Fig. 4);
- a step portion (101) formed in the mounting substrate (101 and 105), at a periphery of the first main surface (see Fig. 4);
- a first conductive pattern (C_1 in the above figure) formed on the first main surface of the mounting substrate (101 and 105) located inside the step portion (see e.g., Fig. 4);
- a second conductive pattern (112) formed on the second main surface of the mounting substrate (see Fig. 4);
- a semiconductor element (121) fixed to the first main surface of the mounting substrate and electrically connected (by wire 106) to the first conductive pattern (C_1); and
- sealing resin (103; column 1, line 35) covering the first main surface of the mounting substrate and the step portion to seal the semiconductor element (see Fig. 4),

- wherein a side surface (S in the figure of the previous page) of the sealing resin (103) and a side surface of the mounting substrate (105) are located on a same plane (see the figure in the previous page).

Regarding claims 2 and 9, Takeda discloses in e.g., Fig. 4 the first conductive pattern (C_1) comprising a bonding pad (the bonding area of C_1 that is bonded to the wire 106) electrically connected to the semiconductor element (121) through a fine metallic wire (106) and a plating line (P_1) extending from the bonding pad to the step portion. Furthermore, the term "plating" is a process designation, and would thus not carry patentable weight in this claim drawn to a product. See In re Thorp, 227 USPQ 964 (Fed. Cir. 1985).

Regarding claims 3 and 10, Takeda discloses in e.g., Fig. 4 a plurality of the bonding pads (the bonding areas of C_1 that are bonded to the wire 106) being arranged so as to surround the semiconductor element (121; see Fig. 4), further comprising a wiring portion (WP_1; see the figure in the previous page) extending from each of the plurality of bonding pads under the semiconductor element (see Fig. 4).

Regarding claims 6 and 11, Takeda discloses in e.g., Fig. 4 the mounting substrate (101 and 105) comprising a resin (Since the substrate 101 and 105 includes mounting portion 101 which is made by epoxy resin, the substrate 105 comprises a resin material; column 1, lines 34 and 35).

Regarding claims 7 and 12, Takeda discloses in e.g., Fig. 4 the second conductive pattern comprising electrodes (112) arranged in a matrix (see Fig. 4).

Regarding claim 8, Takeda discloses in e.g., Fig. 4 a semiconductor device (the device in Fig. 4), comprising:

- a mounting substrate (101 and 105; see Fig. 4 and column 1, lines 33 – 38) having a first main surface (the surface where the sealing resin 103 are formed) and a second main surface (the surface where the sealing resin 103 are not formed) opposite the first main surface (see Fig. 4);
- a step portion (101) formed a periphery of the first main surface of the mounting substrate (101 and 105; see Fig. 4);
- a first conductive pattern (C_1 in the above figure) formed on the first main surface of the mounting substrate (101 and 105) located inside the step portion (see e.g., Fig. 4);
- a second conductive pattern (112) formed on the second main surface of the mounting substrate (see Fig. 4);
- a semiconductor element (121) fixed to the first main surface of the mounting substrate and electrically connected (by wire 106) to the first conductive pattern (C_1); and
- sealing resin (103; column 1, line 35) covering the first main surface of the mounting substrate and the step portion to seal the semiconductor element (see Fig. 4),
- wherein an external side surface of the sealing resin (103) and a side surface of the mounting substrate (101 and 105) are located on a "substantially" same plane (see Fig. 4).

Response to Arguments

6. Applicant's arguments filed on March 6, 2006 have been fully considered but they are not persuasive.

On page 6, applicant argues "claim 1 now recites a step portion that is formed in the mounting substrate ... The Takeda patent neither discloses nor suggests that feature." This argument is not persuasive. Takeda clearly shows in Fig. 4 a step portion (101) that is formed in the mounting substrate (101 and 105), as set forth in the newly amended claim 1 (see paragraph five of this Office action for detail).

For the above reasons, the rejection is maintained.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

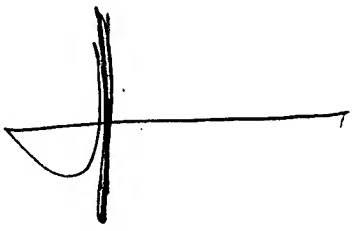
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chris C. Chu
Examiner
Art Unit 2815

c.c.
Tuesday, May 16, 2006



KENNETH PARKER
SUPERVISORY PATENT EXAMINER